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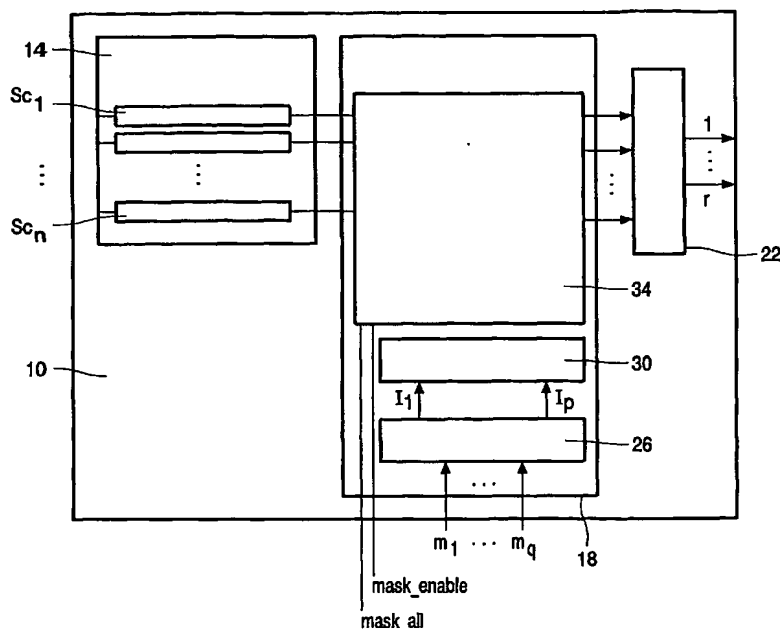
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(54) Title: METHOD AND SYSTEM FOR SELECTIVELY MASKING TEST RESPONSES



(57) Abstract: An apparatus for testing an integrated circuit (10) that comprises a compactor (22) to compress test responses from a circuit-under-test (14) that is part of an integrated circuit (10), and masking circuitry (18) coupled between the circuit-under-test and the compactor (22) for masking one or more of the test responses from the circuit-under-test (14). The masking circuitry (18) further comprises decompression circuitry for receiving compressed mask data and providing decompressed mask data.



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